REMARKS

Reconsideration of the above-identified patent application is requested in view of the remarks that follow.

In the February 12, 2004, Final Rejection, the Examiner rejected claims 77-81, 84 and 85 under 35 U.S.C. 103(a) as being unpatentable over the Igarishi et al. reference in view of the Lin reference and the Tsukamoto reference and the Kata et al. reference. Claim 82 was rejected under 35 U.S.C. 103(a) as being unpatentable over Igarishi et al. in view of Lin and Tsukamoto and Kata et al. and further in view of the Pasch reference. Claim 83 was rejected under 35 U.S.C. 103(a) as being unpatentable over Igarishi et al. in view of Lin and Tsukamoto and Kata et al. and further in view of the Knapp et al. reference.

On April 12, 2004, Applicant filed a response to the Final Rejection. The response set forth, it is believed, sufficient reasons to patentably distinguish claims 77-85 from the reference combinations cited by the Examiner against the respective claims.

On April 28, 2004, the Examiner issued an Advisory Action stating that the April 12, 2004, response had been considered, but that the arguments set forth therein "do not overcome the rejection of record."

Applicant now files a Request for Continued Examination (enclosed herewith) to provide a new opportunity to set forth reasons why Applicant is of the firm and good faith belief that the semiconductor integrated circuit wafer structure disclosed by applicant is patentable over the prior art. Applicant has also amended the claims in this application in a further good faith attempt to clarify the invention.

Reconsideration of new claims 86-94 is requested in view of the following remarks.

Applicant notes several features of the semiconductor integrated circuit wafer structure recited in each of new independent claims 86, 93 and 94 that, it is believed, distinguish the present invention from the structures arrived at by the Examiner in the cited reference combinations.

Each of new independent claims 86, 93 and 94 recites "a unitary, substantially planar solid glass sheet" with "the upper surface of the solid glass sheet being substantially coplanar with the lower surface of the solid glass sheet" and wherein "adhesive material disposed between the upper surface of the substrate wafer and the lower surface of solid glass sheet" affixes "the solid glass sheet to the wafer substrate."

Thus, each of these new claims recites a "unitary" glass sheet that is "solid" and has an upper surface and a lower surface that are "substantially coplanar" and that is "substantially the same size" as the substrate wafer. The specification of the application makes it perfectly clear to a person skilled in the art that these recited features of the glass sheet claim element exist before the glass sheet is affixed to the wafer substrate. Thus, well-established claim construction principles require that this language be interpreted in this way. That is, each of claims 86, 93 and 94 should be interpreted as including a glass sheet that is solid, has substantially coplanar upper and lower surfaces and is of substantially the same size as the substrate wafer before the glass sheet is affixed to the substrate wafer.

The Examiner cites "prefabricated sheet 24" of the Igarishi et al. reference as teaching the glass sheet recited in Applicant's claims. However, as noted by the Examiner, the sheet 24 disclosed by Igarishi et al. is die size, not the wafer size glass sheet recited in Applicant's claims. Furthermore, in contrast to the glass sheet recited in Applicant's claims, the sheet 24 disclosed by Igarishi et al. is not a "unitary solid" having "coplanar upper and lower surfaces" prior to contact with the integrated circuit die 1. Rather, nothing in the Igarishi et al. reference teaches or suggests that the sheet 24 is formed in any but the conventional way, e.g. using well-known spin-on techniques. In fact, as previously noted by Applicant, Kata et al. specifically discloses utilization of spin-on techniques.

The Examiner then relies on the teaching of the Kata et al. reference in an attempt to extrapolate the "die size" teaching of Igarishi et al. to the wafer scale of Applicant's invention. However, Applicant has found nothing in the Kata et al. disclosure that either teaches or suggests a glass sheet that is a unitary solid having substantially coplanar upper and lower surfaces prior to affixation to a substrate wafer, as recited in Applicant's new claims 86, 93 and 94.

Each of Applicant's new independent claims 86, 93 and 94 also recites that "the holes in the glass sheet are prefabricated prior to affixation of the solid glass sheet to the wafer substrate." This feature of the invention also clearly described in Applicant's specification.

Since, as discussed above, the film elements of the Igarishi et al. reference and the Kata et al. reference that are relied upon by the Examiner as being comparable to Applicant's recited glass sheet do not exist as a solid glass sheet of the type recited in Applicant's claims prior to their formation on the IC die (Igarishi et al.) or the wafer (Kata et al.), the hole patterns in these film elements are not "prefabricated prior to affixation of the solid glass sheet to the wafer substrate" as recited in Applicant's new independent claims 86, 93 and 94.

For the reasons set forth above, Applicant is of the good faith belief that all claims now present in this application patentably distinguish over the prior art. Therefore, it is requested that this application be passed to allowance.

Respectfully submitted,

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